SANJEEV AGRAWAL GLOBAL EDUCATIONAL (SAGE) UNIVERSITY, BHOPAL

MTech (VLSI DESIGN & EMBEDDED SYSTEM)

Program Structure

Program Educational Objectives (PEOs)

- **PEO-1:** To prepare the students with good understanding of the respective subjects with design, analytical and problem solving skills.
- **PEO-2:** To train the students with knowledge of latest design trends.
- **PEO-3:** To inculcate in students the sense of ethics, morality, professionalism, creativity, leadership, independent thinking, self confidence, good communication skills and prepare them to become successful engineers who can work worldwide in industries and research & development laboratories.
- **PEO-4:** To introduce the research world to them so that they feel motivated for higher studies and innovation not only in their own domain but multidisciplinary domain.
- **PEO-5:** To recognize social needs and contribute effectively through self learning.

Program Outcome (POs):-

- **PO-1:** The graduates will be able to apply the concepts of Engineering mathematics through Laplace, z-transform, linear algebra, probability and statistics, differential equations etc. and basic knowledge of engineering physics and chemistry.
- **PO-2:** The graduates will be able to understand, interpret the problem, design and perform the experiments to meet the desired solution of the problem within the context of electronics and communication engineering.
- **PO-3:** The graduates will have a good understanding of professional and ethical responsibility.
- **PO-4:** The graduates will be able to express themselves effectively through written and oral communication.

- **PO-5:** The graduates will have a good understanding and knowledge in applying the engineering solutions to society.
- **PO-6:** The graduates will have a good understanding for the need of life long learning and will be able to work in teams.
- **PO-7:** The graduates will show good proficiency in applying the techniques and knowledge of modern engineering skills in tackling contemporary technological challenges.
- **PO-8:** The graduates will have good background for admission to post graduate programs (in same domain), management degree programs and also research programs in various organizations of national and international repute.
- **PO-9:** The graduates will be able to participate and succeed in competitive examinations.
- **PO-10:** Adapt transform in industry by understanding the need of independent and lifelong learning.

M Tech (VLSI DESIGN & EMBEDDED SYSTEM)

First Year – Semester First																
Course Code	**Course Title**	**Contact Hours per Week**			**Credits**	**ETE Duration (Hours)**	**Theory**						**Practical**			
		L	**T**	**P**			**MSE**	**ASG**	**TA**	**ATTD**	**ESE**	**Total**	**CE**	**ESE**	**Total**	**Grand Total**
VE22M101	VLSI Technology and Design	3	1	-	4	3	30	05	05	10	50	100	-	-	-	100
VE22M102	CPLD and FPGA Architectures	3	1	-	4	3	30	05	05	10	50	100	-	-	-	100
VE22M103	Embedded Systems-I	3	1	-	4	3	30	05	05	10	50	100	-	-	-	100
	DSE – I	3	-	-	3	3	30	05	05	10	50	100	-	-	-	100
	DSE – II	3	-	-	3	3	30	05	05	10	50	100	-	-	-	100
VE22M104	Digital VLSI Design Lab	-	-	4	2	2	-	-	-	-	-	-	20	30	50	50
VE22M105	Embedded Systems Lab-I	-	-	4	2	2	-	-	-	-	-	-	20	30	50	50
PB22M101	Project Based Learning-I	-	-	4	2		-				-	-	50	50	100	100
VE22M106	Electronic Device Automation	-	-	4	2	2	-				-	-	20	30	50	50
-	-	**Total**			26	-	-					500			250	750

MSE- Mid Semester Exam, ASG- Assignment, TA- Teacher's Assessment, ATTD-Attendance, ESE- End Sem Exam, CE- continuous Evolution

M Tech (VLSI DESIGN & EMBEDDED SYSTEM)

First Year – Semester Second																
Course Code	**Course Title**	**Contact Hours per Week**			**Credits**	**ETE Duration (Hours)**	**Theory**						**Practical**			
		L	**T**	**P**			**MSE**	**ASG**	**TA**	**ATTD**	**ESE**	**Total**	**CE**	**ESE**	**Total**	**Grand Total**
VE22M201	Embedded Systems-II	3	1	-	4	3	30	05	05	10	50	100	-	-	-	100
VE22M202	Low Power VLSI Design	3	1	-	4	3	30	05	05	10	50	100	-	-	-	100
VE22M203	Analog IC Design	3	1	-	4	3	30	05	05	10	50	100	-	-	-	100
	DSE – III	3	-	-	3	3	30	05	05	10	50	100	-	-	-	100
	DSE – IV	3	-	-	3	3	30	05	05	10	50	100	-	-	-	100
VE22M204	Analog IC Design lab	-	-	4	2	3	-	-	-	-	-	-	20	30	50	50
PB22M201	Project Based learning-II	-	-	4	2	-	-				-	-	50	50	100	100
VE22M205	Embedded Systems Lab-II	-	-	4	2	-	-				-	-	20	30	50	50
-	-	Total			24	-	-					500			200	700

Second Year – Semester Third																
Course Code	**Course Title**	**Contact Hours per Week**			**Credits**	**ELTE**	**Theory**						**Practical**			
		L	**T**	**P**			**MSE**	**ASG**	**TA**	**ATTD**	**ESE**	**Total**	**CE**	**ESE**	**Total**	**Grand Total**
MO22M301	MOOC-1	-	-	8	4	-	-	-	-	-	-	-	50	50	100	100
MO22M302	MOOC - 2	-	-	8	4	-	-	-	-	-	-	-	50	50	100	100
VE22M303	Dissertation Phase-I	-	-	24	12	2	-				-	-	150	150	300	300
-	-	**Total**			20		-					-	-		-	500

MSE- Mid Semester Exam, ASG- Assignment, TA- Teacher's Assessment, ATTD-Attendance, ESE- End Sem Exam ,CE- continuous Evolution

Second Year – Semester Fourth																
Course Code	**Course Title**	**Contact Hours per Week**			**Credits**	**ETE Duration (Hours)**	**Theory**						**Practical**			
		L	**T**	**P**			**MSE**	**ASG**	**TA**	**ATTD**	**ESE**	**Total**	**CE**	**ESE**	**Total**	**Grand Total**
VE22M401	Dissertation Phase-II	-	-	32	16	2	-				-	-	250	250	500	500
-	-	**Total**			16		-					-	-		-	500

MSE- Mid Semester Exam, ASG- Assignment, TA- Teacher's Assessment, ATTD-Attendance, ESE- End Sem Exam, CE- continuous Evolution

Master of Technology (VLSI DESIGN & EMBEDDED SYSTEM)

2 Years Degree Program

Curriculum Components

Components	Credits
Program Core (11 Courses)	**34**
Program Electives (Discipline Specific Electives) (04Courses)	**12**
Project Based Learning (PBL) (02 courses)	**04**
MOOCs (02 courses)	**08**
Dissertation (02 Courses)	**28**
Total	**86**

Distribution of credits across all components

SEM No.	Programme Core	Discipline Specific Electives (DSE)	Project Based Learning (PBL)	MOOCs	Dissertation	Total Credit
I.	18	6	2		-	**26**
II.	16	6	2		-	**24**
III.	-	-		8	12	**20**
IV.	-	-		-	16	**16**
Total	**34**	**12**	**4**	**08**	**28**	**86**

MTech (VLSI DESIGN & EMBEDDED SYSTEM)

List of Program Discipline Specific Electives (DSE)

First Year – Semester One (DSE-I)		
SN	**Course Code**	Course Title
1.	VE22M107	Advanced Digital Signal Processing
2.	VE22M108	Design for Testability
3	VE22M109	CMOS RF Circuit Design
First Year – Semester One (DSE-II)		
SN	Course Code	Course Title
1.	VE22M110	Device Modelling
2.	VE22M111	Real Time Embedded System
3	VE22M112	Advanced logic design
First Year – Semester Second-(DSE-III)		
SN	Course Code	Course Title
1.	VE22M206	CMOS mixed signal circuit design
2.	VE22M207	Embedded Networking
3.	VE22M208	Digital System Design
First Year – Semester Second-(DSE-IV)		
1	VE22M209	Embedded LINUX
2	VE22M210	System on Chip Design
3	VE22M211	Semiconductor Memory Design and Testing

Sanjeev Agrawal Global Educational (SAGE) University, Bhopal

Syllabus

For

M.Tech

VLSI DESIGN & EMBEDDED SYSTEM

I Semester

School of Engineering & Technology

Code	VLSI Technology and Design	Total Lecture:45 Tutorial:15
VE22M101	3 – 1 – 0 = 4	

Course Objectives

- To introduce microelectronics and MOS technologies.
- To realize importance of layout design and tools.
- To study combinational logic networks.
- To learn sequential systems.
- To nurture students with floor planning methods.

Unit	Contents	Hours
1	REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, MOS Transistor circuit model, Latch-up in CMOS circuits.	8
2	LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. LOGIC GATES & LAYOUTS:Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.	10
3	COMBINATIONAL LOGIC NETWORKS:Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.	10
4	SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.	10
5	FLOOR PLANNING: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.	07

Course Outcomes	
At the end of the course the students should be able to:	
CO 1	**Define**[1] The microelectronics and introduction to MOS technologies.
CO 2	**Analyse**[4] The layout design and tools of transistor and logic gates.
CO 3	**Design**[6] The analog & digital CMOS circuits for specified applications.
CO 4	**Explain**[2] The Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families.
CO 5	**Describe**[2] The operation of combinational circuits, sequential circuits and floor planning methods.
Text Books	• Eshraghian. K, Pucknell D, A, (2005), **Essentials of VLSI Circuits and Systems**, PHI. • Prasad K.V.K.K, Kattula Shyamala, 2012, **VLSI Design**, Learning Solutions Inc. • Wayne Wolf, 1997, **Modern VLSI Design**, Pearson Education.
Reference Books	• Ming-BO, 2011, Lin**,Introduction to VLSI Systems: A Logic, Circuit and System,** Perspective, CRC Press, . • Randall L.Geiger, Phillip E.Allen, Noel R.Strader, 2010, **VLSI Design Technologies for Analog and Digital Circuits**, TMH Publications. • Weste N.H.E, Eshraghian. K, **Principals of CMOS VLSI Design**, Addison Wesley.

Code	CPLD and FPGA Architectures	Total Lecture:45 Tutorial: 15
VE22M102	3 – 1 – 0 = 4	

Course Objective-

- To introduce Programmable Logic Devices.
- To make students familiar with FPGA/CPLD Architectures.
- To study finite state machines (FSM).
- To make students aware of FSM Architectures
- To learn System Level Design.

Unit	Contents	Hours
1	Programmable Logic Device And Complex Programmable Logic Devices (CPLD): ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic – 10000 series CPLD, AMD's – CPLD (Mach 1 to 5); Cyprus FLASH 370 Device Technology, Lattice LSI's Architectures – 3000 Series – Speed Performance and in system programmability. Field Programmable Gate Arrays (FPGA) Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs.	10
2	FPGA/CPLD Architectures: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1, 2, 3 and their speed performance.	7
3	Finite State Machines (FSM): Top Down Design – State Transition Table, state assignments for FPGAs. Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL. Alternative realization for state machine chart using microprogramming. Linked state machines. One – Hot state machine, Petrinets for state machines – basic concepts, properties, extended petrinets for parallel controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.	10
4	Fsm Architectures: Architectures centered around non-registered PLDs. State machine designs centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. Application of One – Hot method.	8

5	System Level Design: Controller, data path and functional partitions, Parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.	10
	Course Outcomes	
	At the end of the course the students should be able to:	
CO 1	**Discover**[1] Knowledge about various architectures and device technologies of PLD's.	
CO 2	**Interpret**[3] FPGA Architectures.	
CO 3	**Describe**[2] FSM and different FSM techniques like petrinets & different case studies.	
CO 4	**Explain**[2] FSM Architectures and their applications.	
CO 5	**Analyze**[4] System level Design and their application for Combinational and Sequential Circuits.	
Text Books	• Chan. P. K. and Mourad. S, (1994), **Digital Design Using Field Programmable Gate Array**, Prentice Hall (Pte). • Brown.S., Francis.R., RoseJ., Vransic. Z, (1992), **Field Programmable Gate Array**, Kluwer Publications.	
Reference Books	• Old Field. J, Dorf. R., (1995), **Field Programmable Gate Array**s, John Wiley & Sons, New York. • Trimberger. S., (1994), **Field Programmable Gate Array Technology**, Kluwer Academic Publications. • Bob Zeidman, (2002), **Designing with FPGAs & CPLDs**, CMP Books.	

Code	Embedded Systems	Total Lecture:45 Tutorial: 15
VE22M103	3 – 1 – 0 = 4	

Course Objective:

- To learn about embedded system.
- To study 8051 micro-controller.
- To analyze 8051 micro-controller instruction set and addressing modes.
- To introduce 8051 Interfacing and Applications.
- To make students familiar with different advanced micro-controllers.

Unit	Contents	Hours
1	Introduction to Embedded system, Embedded System Project Management, ESD and CO design issues in System development Process, Design cycle in the development phase for an embedded system, Use of target system or its emulator and In-circuit emulator, Use of software tools for development of an ES.	10
2	8051 Micro-controller: Microprocessor V/s Micro-controller, 8051 Micro-controller: General architecture; Memory organization; I/O pins, ports & circuits; Counters and Timers; Serial data input/output; Interrupts.	10
3	8051 Instructions: Addressing Modes, Instruction set: Data Move Operations, Logical Operations, Arithmetic Operations, Jump and Call Subroutine, Advanced Instructions.	9
4	8051 Interfacing and Applications: Interfacing External Memory, Keyboard and Display Devices: LED, 7-segment LED display, LCD.	8
5	Advanced Micro-controllers: Only brief general architecture of AVR, PIC and ARM micro-controllers; JTAG: Concept and Boundary Scan Architecture.	8
	Course Outcomes	
	At the end of the course the students should be able to:	
CO 1	**Label**[1] and list the signals, architecture of micro-controller, interfacing devices and embedded systems.	

CO 2	**Understand**[2] The operations, internal functions of micro-controller, interfacing circuit and characteristic details of embedded systems architectures.	
CO 3	**Describe**[2] The architecture of 8051 micro-controller.	
CO 4	**Develop**[3] The circuit and demonstrate programming proficiency for interface the micro-controller with external devices.	
CO 5	**Analyse**[4] The operation of advanced micro-controllers.	
Text Books	• Raj Kamal, (2006), **Embedded Systems** TMH, • Ayala. K, (2007), **The 8051 Micro-controller**, 3rd Ed., Thomson Delmar Learning. • Ghoshal. S, (2010), **8051 Micro-controller**, Pearson Education. • Uma Rao. K and Pallavi. A, (2009), **The 8051 Micro-controllers** by Pearson Ed.	
Reference Books	• Raj Kamal, (2005), **Micro-controllers**, Pearson Education. • Huang H.W, (2007), **PIC Micro-controlle**r, Delmar CENGAGE Learning,. • Peatman J. B, (1997), **Design with PIC Micro-controllers**, Prentice Hall.	

Code	Digital VLSI Design Lab	Total Lecture:30
VE22M104	**List Of Experiments**	**0– 0– 2 = 2**
1	Design CMOS Inverter.	
2	Design CMOS AND Gate.	
3	Design CMOS OR Gate.	
4	Design CMOS NAND Gate.	
5	Design CMOS EX-OR Gate.	
6	Design CMOS EX-NOR Gate	
7	Design SR NAND Latch.	
8	Design SR NOR Latch.	
9	Design CMOS Invert Layout.	
10	Design CMOS NOR Gate	

Code	Embedded System-I Lab 1	Total Lecture:30
VE22M105	**List Of Experiments**	**0– 0– 2 = 2**
1	Design With 8 bit Microcontrollers 8051 pic micro controllers-Assembly and C Programming: IO Programming. Timers.	
2	Interrupts: Serial port programming with 8051 PIC microcontrollers. Assembly and C Programming.	
3	PWM Generation Motor Control: ADC DAC with 8051 PIC Micro-controllers-Assembly and C programming.	
4	LCD and RTC interfacing: Sensor Interfacing 8051 PIC Micro-controllers-Assembly and C Programming.	
5	Design with 16-bit Processors: Timers, Interrupts, Serial Communication.	
6	Design with ARM Processors: I\O Programming, ADC DAC,Timers, Interrupts.	
7	Study of one type of real time Operating system (RTOS).	
8	Simple wired wireless network simulation using NS2 Software.	
9	Programming of TCP IP protocol stack.	

Code	Electronic Design Automation Lab	Total Lecture:30
VE22M106	**List of Experiments**	**0– 0– 2 = 2**
1	Write the Code using VERILOG, Simulate and synthesize the following 1. Arithmetic Units: Adders and Subtractors.	
2	Write the Code using VERILOG, Simulate and synthesize Multiplexers and Demultiplexers.	
3	Write the Code using VERILOG, Simulate and synthesize Encoders, Decoders, Priority Encoder and Comparator.	
4	Write the Code using VERILOG, Simulate and synthesize 8-bit parallel adder using 4-bit tasks and functions.	
5	Write the Code using VERILOG, Simulate and synthesize Arithmetic and Logic Unit with minimum of eight instructions.	
6	Write the Code using VERILOG, Simulate and synthesize Flip-Flops.	
7	Write the Code using VERILOG, Simulate and synthesize Registers.	
8	Write the Code using VERILOG, Simulate and synthesize Sequence Detector using Mealy type state machines.	
9	Write the Code using VERILOG, Simulate and synthesize Sequence Detector using Moore type state machines.	
10	Write the Code using VERILOG, Simulate and synthesize Counters.	

Code	Discipline Specific Elective- I	Total Lecture:45
VE22M107	Advanced Digital Signal Processing	Total Lecture:45
		3 – 0 – 0 = 3

Course Objective:

- To make students familiar with the most important methods in DSP
- To introduce students with Overview of the signal processing of Deterministic signals
- To introduce students with the Including digital filter design,
- To introduce students with the Transform-domain processing and importance of Signal Processors.
- To make students aware about the meaning and implications of the properties of systems and signals

Unit	Contents	Hours
1	Overview of the signal processing of Deterministic signals: Time domain and frequency domain response of the linear-shift invariant systems..	12
2	IIR Filter Design: Filter Approximation, Impulse Invariant Method, Bi-linear Transformation method filter structures, Finite word length effects, limitations of IIR filters. FIR Filter Design: Linear phase response, Windowing technique, Gibb's Phenomenon, Frequency Sampling Method, FIR Filter structures.	12
3	Power Spectrum Estimation, Classical Spectral Estimation, Non parametric methods for power spectrum estimation: Bartlet method, Welch method, Blackman and Tuckey method, performance analysis of various techniques.	12
4	Parametric Modeling - AR, MA, ARMA methods, Minimum variance spectral estimations. Filter Bank methods.	9
	Course Outcomes	
	At the end of the course the students should be able to:	

CO 1	**Understand**[2] Use concepts of trigonometry, complex algebra, Fourier transform, z-transform to analyze the operations on signals and acquire knowledge about Systems.	
CO 2	**Remembering** [1] Select proper tools for analog-to-digital and digital-to-analog conversion. Also select proper tools for time domain and frequency domain implementation.	
CO 3	**Creating**[6] The Design, implementation, analysis and comparison of digital filters for processing of discrete time signals.	
CO 4	**Apply**[3] Integrate computer-based tools for engineering applications.	
CO 5	**Creating**[6] The Employ signal processing strategies at multidisciplinary team activities. . Assess the techniques, skills, and modern engineering tools necessary for analysis of different electrical signals and filtering out noise signals in engineering practice.	
Text Books	• Proakis.G. J and Manolakis D. G, **Digital Signal Processing**, **Principles, Algorithms andApplications**, 4th ed. Pearson Education. • S. K. Mitra, **Digital Signal Processing,** 3rd ed. TMH.	
Reference Books	• A.V. Oppenheim and R.W. Schafer, (1992), **Discrete Time Signal Processing**, PHI . • Steven M. Kay, (1988), **Modern Spectral Estimation**, PHI . • Clark Cory.L, (2005), Lab view DSP and Digital comm, TMH. • Roman Kuc, (1988), Introduction to Digital Signal Processing, McGraw Hill.	

Code	Discipline Specific Elective- II	Total Lecture:45
VE22M108	**Design For Testability**	**3 – 0 – 0 = 3**

Course Objective-

- To introduce Philosophy and role Testing.
- To study about Logic and Fault Simulation.
- To make students aware about Testability Measures.
- To learn about Built-In Self-Test.
- To make students familiar about Boundary Scan Standard.

Unit	Contents	Hours
1	Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.	10
2	Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.	10
3	Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.	10
4	Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.	8
5	Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.	7

Course Outcomes		
At the end of the course the students should be able to:		
CO 1	**Identify**[2] The problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs	
CO 2	**Understand**[2] The Simulation for Design Verification, Test Evaluation and Fault Simulation.	
CO 3	**Analyze4** The various Trade-Offs and Techniques for Test ability.	
CO 4	**Explain2** The concepts of built-in-self-test II.	
CO 5	**Illustrate3** The Boundary Scan Standard.	
Text Books	• Bushnell M. L, Agrawal V. D, (2005), **Essential of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits**, Kluwer Academic Publishers. • Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, (2001), **Digital Systems Testing and Testable Design**, Jaico Publishing House. • Alfred Crouch, **Design for Test for Digital ICs & Embedded Core Systems**, Prentice Hall.	
Reference Books	• Englehood Cliffs, Robert J. Feugate, Jr., Steven M.Mentyn, (1998), **Introduction to VLSI Testing**, Prentice Hall. • Lala P. K, **Digital Circuits Testing and Testability**, Academic Press. • Robert J.Feugate, Jr., Steven M.Mentyn, (1998), **Introduction to VLSI Testing**, PHl, Englehood Cliffs.	

Code	Discipline Specific Elective- I	Total Lecture:45 Tutorial: 00
VE22M109	CMOS RF Circuit Design	3 – 0 – 0 = 3

Course Objective :

- To introduce RF Design and Wireless Technology.
- To learn about RF Modulation: Analog and digital modulation of RF circuits.
- To make students aware about RF Testing.
- To study about BJT and MOSFET behavior at RF Frequencies.
- To make students familiar with RF Circuits Design:

Unit	Contents	Hours
1	Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Inter symbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion	8

2	RF Modulation: Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, Direct conversion and two-step transmitters	10
3	RF Testing: RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.	7
4	BJT and MOSFET behavior at RF Frequencies: BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation	10
5	RF Circuits Design: Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Design issues in integrated RF filters.	10

Course Outcomes

At the end of the course the students should be able to:

CO 1	**Understand**[2] The RF Design and Wireless Technology.	
CO 2	**Analyze**[4] The Analog and digital modulation of RF circuits.	
CO 3	**Discuss**[2] The RF testing for heterodyne, Homodyne	
CO 4	**Explain**[2] The BJT and MOSFET behavior at RF Frequencies.	
CO5	**Design**[6] The RF filters circuit.	
Text Books	• Razavi. B, (1998), **RF Microelectronics**, PHI. • Jacob Baker. R, Li H.W, Boyce D.E, (2007), **CMOS Circuit Design, layout and Simulation**, PHI.	

	• Bowick, (2007), **RF Circuit Design**, 2nd Edition, Newnes.
Reference Books	• Thomas H. Lee, (1998), **Design of CMOS RF Integrated Circuits**, Cambridge University press. • Tsividis Y.P, (1996), **Mixed Analog and Digital Devices and Technology**, TMH. • Ludwig, (2011), **RF Circuit Design Theory And Application**, Pearson.

Code	Discipline Specific Elective- II	Total Lecture:45
VE22M110	Device Modelling	3 – 0 – 0 = 3

Course Objective:

- To make students familiar with MOS Capacitor
- To learn MOS Characteristics and Non idealities.
- To study about Small signal modeling for low frequency and High frequency
- To introduce The bipolar transistor and
- To make students aware about FinFETs and VI Characteristics.

Unit	Contents	Hours
1	MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Mid gap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation.	10
2	MOS Capacitor Characteristics and Non idealities: CV characteristics of MOS, LFCV and HFCV, Non idealities in MOS, oxide fixed charges, interfacial charges.	8
3	The MOS transistor: Small signal modeling for low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors.	7
4	The bipolar transistor: Eber's-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics. Signal-space dimensionality and processing gain	10
5	FinFETs: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.	10

Course Outcomes

At the end of the course the students should be able to:

CO 1	**Extend**^{2} The depth knowledge in various characteristics of MOS Transistors.	

CO 2	**Analyze**[4] The complex MOS device structures.	
CO 3	**Design**[6] The engineering problems with wide range of solutions in different MOSFET technologies.	
CO 4	**Identify**[1] The characteristic of MOSFET in dynamic operation	
CO 5	**Apply**[3] The appropriate techniques, resources and tools to engineering activities in modeling MOS structures.	
Text Books	• Sze. S. M, (1981), **Physics of Semiconductor Devices**, 2nd Edition, Wiley Eastern, • Tsividis. Y. P, (1987), **Operation and Modelling of the MOS Transistor**, McGraw-Hill. • Nandita Das Gupta and Amitava Das Gupta, **Semiconductor Devices**, PHI.	
Reference Books	• Takeda. E, (1995), **Hot-carrier Effects in MOS Transistors**, Academic Press. • Colinge. P, (2009), **FinFETs and Other Multi-Gate Transistors**, Springer. • S. Tyagi, (2008), **Introduction to Semiconductor Materials and Devices**, Wiley.	

Code	Discipline Specific Elective- II	Total Lecture:45
VE22M111	Real Time Embedded System	3 – 0 – 0 = 3

Course Objectives

This course will enable students to:

- Understand basics of Real Time systems
- Distinguish a real-time system with other systems.
- Identify the functions of operating system.
- Evaluate the need for Real time operating system.
- Design and develop embedded applications by means of real-time operating systems.

Unit	Contents	Hours
1	Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Re-entrant Functions.	10
2	Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonic least upper bound, and Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies. I/O Resources: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture. Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.	10
3	Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion. Soft Real-Time Services: Missed Deadlines, QoS, and Alternatives to rate monotonic policy, Mixed hard and soft real-time services.	10
4	Embedded System Components: Firmware components, RTOS system software mechanisms, Software application components. Debugging Components: Exceptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self-test and diagnostics.	8
5	Performance Tuning: Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length. High availability and Reliability Design: Reliability and Availability,	7

	Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design	

Course Outcomes	
At the end of the course the students should be able to:	
CO 1	**Analyze^4** The Real time operating systems
CO 2	**Understand^2** Describe the functions of Real time operating systems
CO 3	**Understand^2** The Demonstrate embedded system applications
CO 4	**Creating^6** The Design a Real Time operating system
CO 5	**Analyze^4** The performance tuning: basic concepts
Text Books	• Sam Siewert (2007): **Real-Time Embedded Systems and Components** Cengage Learning India Edition
Reference Books	• Krishna CM and Kang Singh G. (2003): **Real time systems**, Tata McGraw Hill. • Qing Li and Carolyn Yao, (2003): **Real-Time Concepts for Embedded Systems**, CMP Books. • Jane W. S. Liu, (2000): **Real Time Systems**, Prentice Hall. • Phillip A. Laplante, (2004): **Real-Time Systems Design and Analysis**, John Wiley & Sons,

Code	Discipline Specific Elective- II	Total Lecture:45
VE22M112	Advanced Logic Design	3 – 0 – 0 = 3

- To Introduce to logic circuit and Verilog.
- To make students familiar about Verilog data types and operators.
- To study Verilog specifications of combinational circuits.
- To learn about Synchronous sequential circuits.

Unit	Contents	Hours
1	Introduction to logic circuit and Verilog, Implementation technology, CMOS logic gates, programmable logic devices. Optimized implementations of logic functions, canonical representations, Karnaugh maps, factoring, functional decomposition, NAND/NOR networks, bubble pushing.	15
2	Verilog data types and operators, modules and ports, gate level modeling, time simulation/ scheduler. Circuit issues. Verilog behavioral models, number representation and arithmetic circuits, positional notation, signed numbers, arithmetic operations.	15
3	Verilog specifications of combinational circuits, combinational logic building blocks, encoders/decoders, arithmetic comparison, etc. The basic latch, gated SR and D latch, master-slave and edge-triggered flip flops, counters, shift registers, Design examples, introduction to finite state machines; introduction to Model Sim.	8
4	Synchronous sequential circuits, design process, state assignment, hazards, glitches, asynchronous design, Metastability, Noise margins, Power, fan-out, skew Finite state machine design examples, Verilog representations.	7

Course Outcomes

At the end of the course the students should be able to:

CO 1	**Define**[1] The role of optimization and ability to apply multi-output and multi-level optimizations in digital circuit design.	

CO 2	**Design**[6] The asynchronous sequential circuits using systematic approaches.	
CO 3	**Explain**[2] the basic process of VLSI testing, stuck-at fault model, fault simulation and the concept of design-for-test methodologies (scan and built-in self-test).	
CO 4	**Analyze**[4] The graph-based algorithms and linear programming for scheduling, binding and resource sharing in high-level synthesis.	
CO 5	**Demonstrate**[2] VHDL/Verilog and CAD tools for optimization, simulation and synthesis	
Text Books	• John F. Wakerly, **Digital Design**, Pearson Education Asia, 3rd Ed. • Mano. M. M, **Digital Design**, Pearson Education, 3rd Ed. • Roth C. H, Jr., **Fundamentals of Logic Design**, Jaico Publishing House. • Fletcher, A**n Engineering Approach to Digital Design**, PHI.	
Reference Books	• Stephen Brown and Zvonko Vranesic, (2003), **Fundamentals of Digital Logic with Verilog Design**, McGraw-Hill Higher Education. • Samir Palnitkar, (2003), **Verilog HDL**, Prentice Hall, 2nd Edition. • Yarbrough J. M, **Digital Logic**, Thomson Learning.	

COURSE CODE	PROJECT BASED LEARNING-I	Total Lecture:30 Practical:30
PB22M101		0-0-4=2
Learning Objectives:	• Integrating the knowledge and skills of various courses on the basis of multidisciplinary projects • Develop the skill of critical thinking and evaluation. • To develop 21st century success skills such as critical thinking, problem solving, communication, collaboration and creativity/innovation among the students. • To enhance deep understanding of academic, personal and social development in students. • Employ the specialized vocabularies and methodologies.	
Course Outcome		
At the end of the course the students will be able to:		
Course Outcomes:	• **Apply**[3]a sound knowledge/skills to select and develop their topicand project respectively. • **Develop**[6] plans and allocate roles with clear lines of responsibilityand accountability. • **Design**[6] solutions to complex problems following a systematic approach like problem identification, formulation and solution. • **Collaborate**[6] with professionals and the community at large in written and in oral forms. • **Correlate**[4]the knowledge, skills and attitudes of a professional.	
General Guidelines:	• PBL will be an integral part of UG/PG Programs at different levels. • Each semester offering PBL will provide a separate Course Code, twocredits will be allotted to it. • Faculty will be assigned as mentor to a group of 30 student's minimum byHoS. • Faculty mentor will have 4 hours/week to conduct PBL for assigned students. • Student will select a topic of their choice from syllabus of any course offered in respective semester (in-lines with sustainable development goals). • Student may work as a team maximum 3 or minimum 2 members for single topic. • For MSE, student's performance will be assessed by panel of three experts either from other department/school, or from samedepartment/school based on chosen topic. This will be comprised of apresentation by student followed by viva-voce. It will be evaluated for 30 marks. • 20 marks would be allotted for continuous performance assessment by concerned guide/mentor. For ESE, student will need to submit a project report in prescribed format, duly signed by concerned guide/mentor and head of the school. The report should be comprised of following components:	

	1. Introduction 2. Review of literature 3. Methodology 4. Result and Discussion 5. Conclusion and Project Outcomes 6. References • Student will need to submit three copies for 1. Concerned School 2. Central Library 3. Self • The integrity of the report should be maintained by student. Any malpractice will not be entertained. • Writing Ethics to be followed by student, a limit of 10 % plagiarism is permissible. Plagiarism report is to be attached along with the report. • Project could be a case study/ analytical work /field work/ experimental work/ programming or as per the suitability of the program.

Sanjeev Agrawal Global Educational (SAGE) University, Bhopal

Syllabus

For

M.Tech

VLSI DESIGN & EMBEDDED SYSTEM

II Semester

School of Engineering & Technology

Code	Embedded System Design-II	Total Lecture:45 Tutorial=15
VE22M201		3 – 1 – 0 = 4

Course Objective-

- To learn about The PIC Microcontroller Architecture.
- To make students aware about PIC hardware features.
- To study programming with PIC.□
- To introduce Hardware Interfacing and Applications:□
- To give overview to students about ARM processor fundamentals.

Unit	Contents	Hours
1	THE PIC MICROCONTROLLER ARCHITECTURE: CPU, ALU , Data Movement, The Program Counter and Stack, Reset , Interrupts, Architecture Differences, Mid-Range instruction Set.	8
2	PIC HARDWARE FEATURES :Power Input and Decoupling , Reset, Watchdog Timer, System Clock/Oscillators, Configuration Registers, Sleep , Hardware and File Registers, Parallel Input Output, Interrupts, Prescaler , The OPTION Register , Mid-Range Built-In EEPROM Flash Access, TMR1 andTMR2 Serial I/0, Analog I/0, Parallel Slave Port (PSP), External Memory Connections, In-Circuit Serial Programming (ISCP).	10
3	PROGRAMMING WITH PIC :Assembly Language Programming, Hex File Format, Code-Protect Features, Programming, PIC Emulators .	7
4	HARDWARE LNTERFACING :Estimating Application Power Requirements, Reset, lnterfacing to External Devices, LEDs, Switch Bounce , Matrix Keypads , LCDs, Analog I/O, Relays and Solenoids, DC and Stepper Motors, Servo Control Serial Interfaces .	10
5	ARM PROCESSOR FUNDAMENTALS: Registers, State and Instruction Sets, Pipeline, Memory Management, Introduction to the ARM Instruction Set.	10

Course Outcomes

	At the end of the course the students should be able to:	

CO 1	**Understand**[2] The PIC MICROCONTROLLER ARCHITECTURE.	
CO 2	**Analyse**[4] The PIC Micro-controller hardware features.	
CO 3	**Demonstrate**[3] The assembly language PROGRAMMING with PIC.	
CO 4	**Discuss**[2] The Hardware Interfacing and its Applications.	
CO5	**Explain**[2] The ARM processor fundamentals.	
Text Books	• Myke Predko, (2007), **Programming and customizing PIC Micro-controller**, Mc- Graw Hill. • Raj Kamal, (2006), **Embedded Systems,** TMH. • Lyla b. das, (2012), **Embedded Systems- An integrated approach**, Pearson education	
Reference Books	• John.B. Peatman, (2003), **Design with PIC Microcontroller**, Pearson Education. • Steave Furber, (2000), **ARM system – on – Chip Architecture**, Addison Wesley. • Shibu. K. V, (2009), **Introduction to Embedded Systems** , Mc Graw Hill Education.	

Code	Low Power VlSI Design	Total Lecture:45 Tutorial: 15
VE22M202	**3 – 1 – 0 = 4**	

Course Objective-

- To introduce basic knowledge of low voltage device modelling
- To provide overview of low voltage, low power VLSI CMOS circuit design
- To familiarize the students with the modelling and simulation
- To provide strong foundation logic synthesis and verification
- To introduce students with the high –level synthesis

Unit	Contents	Hours
1	LOW POWER DESIGN, AN OVER VIEW : Introduction to low – voltage low power design, limitations, silicon –on-Insulator	10
2	GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking branch and bound, Dynamic programming, Integer linear programming, Local search, simulated annealing, tabu search, Genetic Algorithms.	10
3	Layout compaction, Placement, Floor planning and Routing problems, Concepts and algorithms. MODELLING AND SIMULATION: Gate level modelling and simulation, Switch level modelling and simulations.	10
4	LOGIC SYNTHESIS AND VERIFICATION : Basic issues and terminology, Binary decision diagrams, two–level logic synthesis.	8
5	HIGH –LEVEL SYNTHESIS: Hardware models, Internal representation of the input algorithm, Allocation assignment and scheduling, some Scheduling Algorithms, some suspects of Assignment problem, High level transformations.	7
	Course Outcomes	
	At the end of the course the students should be able to:	
CO 1	**Understand**^{2} The low power design and different sources of power dissipation.	
CO 2	**Explain**^{2} The various low power design approaches and techniques.	

CO 3	**Analyze**[4] The various types of low power adders.	
CO 4	**Apply**[3] The different low power techniques for designing multipliers.	
CO 5	**Design**[6] The various Hardware models, Internal representation of the input algorithm.	
Text Books	• Sung-Mo Kang, Yusuf Leblebici, (2011), **CMOS Digital Integrated Circuits: Analysis and Design**, MH Professional Engineering. • Kiat-Seng Yeo, Kaushik Roy, **Low-Voltage, Low-Power VLSI Subsystems**, MH Professional Engineering. • Pal, Ajit, (2015), **Low-Power VLSI Circuits and Systems**, Springer.	
Reference Books	• Sung-Mokang and Yusuf leblebici, (2003), **CMOS Digital ICs**, 3rd edition, TMH. • Parhi, **VLSI DSP Systems**, John Wiley & Sons. • Kaushik Roy, Sharat C. Prasad, (2000), **Low Power CMOS VLSI Circuit Design**, John Wiley & Sons, • Gary K. Yeap, (2002), **Practical Low Power Digital VLSI Design**, Kluwer Academic Press, .	

Code	Analog IC Design	Total Lecture:45 Tutorial: 15
VE22M203		**3 – 1 – 0 = 4**

Course Objective-

- To introduce the basics of MOSFET and its characteristics.
- To analyse the small signal analysis and large signal analysis for single stage amplifiers, differential amplifiers, current sources, current mirrors and frequency response of amplifiers.
- To familiarize the students with the current mirrors and voltage references.
- To provide strong foundation the CMOS Operational Amplifiers.
- To introduce students with the Characterization of comparator, Two-Stage, Open-Loop Comparators.

Unit	Contents	Hours
1	MOS Devices and Modelling: The MOS Transistor, I-V characteristics of MOSFET, MOS Switch, MOS Diode, MOS Active Resistor, MOS Large-Signal Model, other Model Parameters, Small-Signal Model of MOSFET, Sub-threshold MOS Model, Integrated circuit Layout, SPICE Models.	10
2	CMOS Amplifiers: Common Source Amplifier configurations, Differential Amplifiers, Cascade Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.	10
3	Current Mirrors and Voltage References: Current Sinks and Sources, Basic Current Mirrors, Cascode Current Mirrors, Wilson Current Mirror, Current and Voltage References.	10
4	CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.	8
5	Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete Time Comparators.	7
	Course Outcomes	
	At the end of the course the students should be able to:	
CO 1	**Understand**[2] The small and large signal models of MOS transistors.	
CO 2	**Analyse**[4] The operation and behaviour of various analog integrated circuits.	
CO 3	**Explain**[4] The current mirror circuits.	

CO 4	**Design**[6] The analog operational transconductance amplifiers.	
CO 5	**Create**[5] A two stage open loop comparator.	
Text Books	• Phillip E. Allen, Douglas R. Holberg, (2013), **CMOS Analog Circuit Design,** Oxford University Press, 3rd edition. • Behzad Razavi, (2017), **Analog CMOS Integrated Circuits**, McGraw Hill, 2nd Edition. • Kenneth Martin, (2013), **Analog Integrated Circuit Design**,Wiley Publications, 2nd Edition .	
Reference Books	• Paul. R. Gray, Paul. R. Hurst, Stephen H. Lewis and Meyer. R. G, (2010), **Analysis and Design of Analog Integrated Circuits**, John Wiley Publications, 5th Edition. • Sedra and Smith, (2013), **Microelectronic Circuits**, Oxford Publications, 6th Edition.	

Code	Analog IC Design Lab	Practical: 30
VE22M204	**List of Experiments**	**0 – 0– 2= 2**
1	Characterization of NMOS and PMOS transistors for analog figure of merits.	
2	Design of single stage amplifiers (CS, CD and CG).	
3	Design of CMOS current mirrors.	
4	Design of active load single stage amplifiers.	
5	Design of CMOS differential amplifier.	
6	Design of CMOS transconductance amplifiers	
7	Design of a two stage CMOS operational amplifier.	
8	Design of CMOS cascade operation amplifier.	
9	Design of basic feedback circuits.	
10	Design of Band-gap reference circuit.	
Note: Minimum of 10 experiments to be conducted		

Code	Embedded Systems Lab-II	Practical:30
VE22M205	**List of Experiments**	**0 – 0– 4= 2**
1	Design With 8 bit Microcontrollers 8051 pic micro controllers- Assembly and C Programming: IO Programming, Timers.	
2	Interrupts. Serial port programming with 8051 PIC microcontrollers. Assembly and C Programming.	
3	PWM Generation Motor Control. ADC DAC with 8051 PIC Microcontrollers-Assembly and C programming.	
4	LCD and RTC interfacing.Sensor Interfacing 8051 PIC Microcontrollers-Assembly and C Programming.	
5	Design with 16-bit Processors: Timers, Interrupts, Serial Communication.	
6	Design with ARM Processors: I\O Programming , ADC, DAC, Timers, Interrupts.	
7	Simple wired wireless network simulation using NS2 Software.	
8	Programming of TCP IP protocol stack.	

Code	Discipline Specific Elective- III	Total Lecture:45
VE22M206	CMOS Mixed Signal Circuit Design	3 – 0 – 0 = 3

Course Objective-

- To introduce the basics of Switched Capacitor circuits
- To design Phase Locked Loops, Digital to Analog converters, Analog to Digital converters and higher order sampling converters
- To familiarize the students with the phased lock loop (pll): basic pll topology
- To provide strong foundation data converter fundamentals
- To introduce students with the Oversampling Converters

Unit	Contents	Hours
1	Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, switched capacitor integrators first order filters, Switch sharing, biquad filters.	10
2	Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.	10
3	Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.	10
4	Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.	8
5	Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.	7
	Course Outcomes	
	At the end of the course the students should be able to:	
CO 1	**Understand**^{2} The design Switched Capacitor Circuits.	
CO 2	**Explain**^{2} The building blocks of PLL and its operation.	

CO 3	**Apply**[3] The engineering problems related to D/A Converters.	
CO 4	**Apply**[3] The appropriate techniques and tools in development of A/D Converters	
CO 5	**Analyze**[3] The appropriate techniques and Design Over sampling converters.	
Text Books	• Behzad Razavi, (2002), **Design of Analog CMOS Integrated Circuits**, TMH Edition. • Philip E. Allen and Douglas R. Holberg, (2010), **CMOS Analog Circuit Design**, Oxford University Press, International Second Edition/Indian Edition. • David A. Johns,Ken Martin, (2013), **Analog Integrated Circuit Design**, Wiley Student Edition. • Behzad Razavi, (2017), **Analog CMOS Integrated Circuits**, McGraw Hill, 2nd Edn . • Kenneth Martin, (2013), **Analog Integrated Circuit Design**, Wiley Publications, 2nd Edition.	
Reference Books	• Rudy Van De Plassche, (2003), **CMOS Integrated Analog-to- Digital and Digital-to-Analog converters**-Kluwer Academic Publishers. • Richard Schreier, (2005), **Understanding Delta-Sigma Data converters**, Wiley Interscience. • Jacob Baker. R, (2009), **CMOS Mixed-Signal Circuit Design**, Wiley Interscience, . • Gustavsson. M, Wikner. J, and Tan Kluwer, (2000), **CMOS Data Converters for Communication**, Academic Publishers, 1st Edition. • R. Jacob Baker, (2008), **CMOS Mixed-Signal Circuit Design**, Wiley Inter science, IEEE press, 2nd Edition.	

Code	Discipline Specific Elective- III	Total Lecture:45
VE22M207	**Embedded Networking**	3 – 0 – 0 = 3

Course Objective-

- To introduce students with the embedded communication protocols.
- To familiarize the students with the Application Development using USB and CAN bus for PIC microcontrollers.
- To provide strong foundation Application development using Embedded Ethernet for Rabbit processors.
- To introduce students with Wireless sensor network communication protocols.

Unit	Contents	Hours
1	Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming – ISA/PCI Bus protocols – Fire wire.	10
2	USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration – Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction – Frames –Bit stuffing –Types of errors – Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.	10
3	Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.	10
4	Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.	8
5	Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization – Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.	7
	Course Outcomes	
	At the end of the course the students should be able to:	
CO 1	**Understand**[2] The USB and CAN bus for PIC microcontrollers.	

CO 2	**Describe**[2] The embedded communication protocols.	
CO 3	**Understand**[2] The engineering development using Embedded Ethernet for Rabbit processors.	
CO 4	**Analyze**[4] The appropriate techniques wireless sensor network communication protocols	
CO 5	**Design**[6] The appropriate techniques exchanging messages using UDP and TCP	
Text Books	• Frank Vahid, Tony Givargis, (2002), **Embedded Systems Design: A Unified Hardware/Software Introduction**, John & Wiley Publications. • Jan Axelson, (1996), Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port, Penram Publications.	
Reference Books	• Dogan Ibrahim, (2008), **Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series**, Elsevier. • Jan Axelson, (2003), **Embedded Ethernet and Internet Complete**, Penram publications. • Bhaskar Krishnamachari, (2005), **Networking Wireless Sensors,** Cambridge Press.	

Code	Discipline Specific Elective- III	Total Lecture:45
VE22M208	Digital System Design	3 – 0 – 0 = 3

Course Objective-

- To introduce several aspects of digital system concepts like PLAs.
- To introduce the concepts & techniques of testing of digital circuits
- To familiarize the students with the minimization procedures and camp algorithm
- To provide strong foundation PLA design, PLA minimization and folding algorithms
- to introduce students with the Fault Diagnosis in Combinational Circuits

Unit	Contents	Hours
1	**Minimization Procedures and CAMP Algorithm**: Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.	10
2	**PLA Design, PLA Minimization and Folding Algorithms**: Introduction to PLDs, basic configurations and advantages of PLDs, PLA Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm (IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples	10
3	**Design of Large Scale Digital Systems**: Algorithmic state machine charts, Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.	10
4	**Fault Diagnosis in Combinational Circuits**: Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.	8
5	**Fault Diagnosis in Sequential Circuits**: Fault detection and location in sequential circuits, circuit test approach, initial state identification, Homing experiments synchronizing experiments, distinguishing experiment, adaptive distinguishing experiments, machine identification.	7
	Course Outcomes	

	At the end of the course the students should be able to:	
CO 1	**Apply**[3] The various minimization methods for minimizing the switching functions.	
CO 2	**Explain**[2] The minimization and folding algorithms for PLA Design.	
CO 3	**Understand**[2] The various aspects in Large Scale Digital Systems design.	
CO 4	**Analyze**[4] The fault modelling concepts to digital circuits and generate the test patterns.	
CO 5	**Understand**[2] The concepts of fault diagnosis in Sequential Circuits.	
Text Books	• N. N. Biswas, **Logic Design Theory**, PHI. • Z. Kohavi , (2001), **Switching and Finite Automata Theory**, 2nd Edition, TMH. • P. K Lala, (1990), **Digital system Design using PLDs**, Prentice Hall.	
Reference Books	• Charles H. Roth, **Fundamentals of Logic Design**, 5th Ed., Cengage Learning. • Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, **Digital Systems Testing and Testable Design**, John Wiley & Sons Inc.	

Code	Discipline Specific Elective- IV	Total Lecture:45
VE22M209	**Embedded Linux**	**3 – 0 – 0 = 3**

Course Objective-

- To introduce students with the fundamentals of operating systems overview of operating systems
- To introduce the concepts & techniques introduction to embedded Linux embedded Linux
- To familiarize the students with the Linux fundamentals introduction to Linux
- To provide strong foundation board support package and embedded storage
- To introduce students with the Linux serial driver

Unit	Contents	Hours
1	FUNDAMENTALS OF OPERATING SYSTEMS Overview of operating systems – Process and threads – Processes and Programs –Programmer view of processes – OS View of processes – Threads - Scheduling – Non preemptive and preemptive scheduling – Real Time Scheduling – Process Synchronization – Semaphores – Message Passing – Mailboxes – Deadlocks –Synchronization and scheduling in multiprocessor Operating Systems	10
2	LINUX FUNDAMENTALS Introduction to Linux – Basic Linux commands and concepts – Logging in - Shells -Basic text editing - Advanced shells and shell scripting – Linux File System –Linux Programming - Processes and threads in Linux - Inter process communication – Devices – Linux System calls	10
3	INTRODUCTION TO EMBEDDED LINUX Embedded Linux – Introduction – Advantages- Embedded Linux Distributions - Architecture - Linux kernel architecture - User space – Linux start-up sequence - GNU cross platform Tool chain	10
4	BOARD SUPPORT PACKAGE AND EMBEDDED STORAGE Inclusion of BSP in kernel build procedure - The bootloader Interface – Memory Map – Interrupt Management – PCI Subsystem – Timers – UART – Power Management – Embedded Storage – Flash Map – Memory Technology Device (MTD) –MTD Architecture - MTD Driver for NOR Flash – The Flash Mapping drivers – MTD Block and character devices – mtdutils package – Embedded File Systems – Optimizing storage space – Turning kernel memor.	8
5	Linux serial driver – Ethernet driver – I2C subsystem – USB gadgets – Watchdog timer – Kernel Modules – Application porting roadmap - Programming with threads – Operating System Porting Layer – Kernel API Driver - Case studies - RT Linux – u Clinux.	7
	Course Outcomes	

	At the end of the course the students should be able to:	
CO 1	**Understand**[2] The fundamentals of operating systems overview of operating systems.	
CO 2	**Apply**[3] The concepts & techniques of embedded Linux.	
CO 3	**Understand**[2] The Linux fundamentals of Linux.	
CO 4	**Analyze**[4] The strong foundation board support package and embedded storage.	
CO 5	**Create**[6] The Linux serial driver Ethernet driver – I2C subsystem.	
Text Books	• David Barron, (2010), **The World of Scripting Languages**, Wiley Student Edition. • Brent Welch, Ken Jones and Jeff Hobbs., **Practical Programming in Tcl and Tk**, 4th edition. • Larry Wall, Tom Christiansen, John Orwant, **Programming Perl**, 3rd Edition, Oreilly publications • Randal L, Schwartz Tom Phoenix, **Learning PERL**, Oreilly publications.	
Reference Books	• Clif Flynt, (2003), **A Developer's Guide**, Morgan Kaufmann Series.	

Code	Discipline Specific Elective- IV	Total Lecture:45
VE22M210	**System on Chip Design**	**3 – 0 – 0 = 3**

Course Objective-

- To introduce students with the System Architecture, Components of the system and system on chip (SOC) design.
- To familiarize the students with the Processor Selection for SOC.
- To provide strong foundation Memory Design for SOC.
- To introduce students with the inter Connect Architectures of SOC.
- To study Application Studies / Case Studies of SOC Design approach.

Unit	Contents	Hours
1	Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.	10
2	Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.	10
3	Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.	10
4	Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.	8
5	Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression	7
	Course Outcomes	
	At the end of the course the students should be able to:	

CO 1	**Understand**[2] The abstraction in Hardware, SOC of ARM Processor.	
CO 2	**Evaluating** [5] The system on chip RISC Machine, three and five stage Pipeline.	
CO 3	**Explain** [3] The Memory Design for SOC.	
CO 4	**Understand**[2] The Interconnect Customization and Configuration.	
CO 5	**Create**[6] the SOC design approaches and AES algorithm.	
Text Books	• Michael J. Flynn and Wayne Luk, **Computer System Design System-on-Chip**, Wiely India Pvt. Ltd. • Steve Furber, (2000), **ARM System on Chip Architecture,** Addison Wesley Professional.	
Reference Books	• Ricardo Reis, (2004), • **Design of System on a Chip: Devices and Components** – Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM. • Prakash Rashinkar, Peter Paterson and Leena Singh, (2001), **System on Chip verification – Methodologies and Techniques,** Kluwer Academic Publishers.	

Code	Discipline Specific Elective- IV	Total Lecture:45
VE22M211	**Semiconductor Memory Design and Testing**	**3 – 0 – 0 = 3**

Course Objective-

- To introduce students with the Random Access Memory Technologies.
- To familiarize the students with the Non-volatile Memories.
- To provide strong foundation Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance.
- To study Semiconductor Memory Reliability and Radiation Effects.
- To introduce students with the Advanced Memory Technologies and High-density Memory Packing Technologies.

Unit	Contents	Hours
1	Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.	10
2	Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.	10
3	Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory	10
4	Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures.	8
5	Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.	7

	Course Outcomes	
	At the end of the course the students should be able to:	
CO 1	**Analyze**[4] The different types of RAM, ROM designs.	
CO 2	**Design**[6] The RAM, ROM architecture and interconnects.	
CO 3	**Correlate**[4] The different memory testing methods and design for testability.	
CO 4	**Apply**[3] The new developments in semiconductor memory design.	
CO 5	**Understand**[2] The various Advanced and High-density Memory Technologies.	
Text Books	• Ashok K. Sharma, (2002), **Semiconductor Memories Technology**, Wiley. • Ashok K. Sharma, **Advanced Semiconductor Memories – Architecture, Design and Applications**, Wiley. • Chenming C Hu, **Modern Semiconductor Devices for Integrated Circuits**, 1st Ed., Prentice Hall.	
Reference Books	• Belty Prince, **Semiconductor Memory Design Handbook**.	

COURSE CODE	PROJECT BASED LEARNING-I	Total Lecture:30 Practical:30
PB22M201	0-0-4=2	
Learning Objectives:	• Integrating the knowledge and skills of various courses on the basis of multidisciplinary projects • Develop the skill of critical thinking and evaluation. • To develop 21st century success skills such as critical thinking, problem solving, communication, collaboration and creativity/innovation among the students. • To enhance deep understanding of academic, personal and social development in students. • Employ the specialized vocabularies and methodologies.	
Course Outcome		
At the end of the course the students will be able to:		
Course Outcomes:	• **Apply**[3]a sound knowledge/skills to select and develop their topicand project respectively. • **Develop**[6] plans and allocate roles with clear lines of responsibilityand accountability. • **Design**[6] solutions to complex problems following a systematic approach like problem identification, formulation and solution. • **Collaborate**[6] with professionals and the community at large in written and in oral forms. • **Correlate**[4]the knowledge, skills and attitudes of a professional.	
General Guidelines:	• PBL will be an integral part of UG/PG Programs at different levels. • Each semester offering PBL will provide a separate Course Code, twocredits will be allotted to it. • Faculty will be assigned as mentor to a group of 30 students minimum byHoS. • Faculty mentor will have 4 hours/week to conduct PBL for assigned students. • Student will select a topic of their choice from syllabus of any course offered in respective semester (in-lines with sustainable development goals). • Student may work as a team maximum 3 or minimum 2 members for single topic. • For MSE, student's performance will be assessed by panel of three experts either from other department/school, or from samedepartment/school based on chosen topic. This will be comprised of apresentation by student followed by viva-voce. It will be evaluated for 30 marks. • 20 marks would be allotted for continuous performance assessment by concerned guide/mentor. For ESE, student will need to submit a project report in prescribed format, duly signed by concerned guide/mentor and head of the school. The report should be comprised of following components:	

	7. Introduction 8. Review of literature 9. Methodology 10. Result and Discussion 11. Conclusion and Project Outcomes 12. References • Student will need to submit three copies for 1. Concerned School 2.Central Library 3. Self • The integrity of the report should be maintained by student. Any malpractice will not be entertained. • Writing Ethics to be followed by student, a limit of 10 % plagiarism is permissible. Plagiarism report is to be attached along with the report. • Project could be a case study/ analytical work /field work/ experimentalwork/ programming or as per the suitability of the program.

MO22M301/MO22M302	MOOC-1/ MOOC-2	Total Lecture: Practical:60
		(LTP=0-0-8=4)
Learning Objective:	• Integrating the knowledge and skills of various courses available in online mode. • Develop the skills of critical thinking and evaluation. • To make students to learn themselves by choosing the course as per there area of interest.	
	CONTENTS	**HOURS**
General Guidelines:	• This course creates an excellent opportunity for students to acquire the necessary skill set for research, employability through massive open online courses (MOOCs) where the rare expertise of world famous experts from academics and industry are available. • The basket for MOOCs will be a dynamic one, as courses keep on updating with time. • In this semester 8 credits will have to be acquired with online courses (MOOCs). Students will have to complete 2 MOOC's of their choice in the third semester. • The MOOC-1 and MOOC-2 each carries internal marks of 50, which will be attained after he/she gets the MOOC certificate for which he/she got himself/herself enrolled. For end sem evaluation a Viva-Voce examination shall be conducted and it will carried 50 marks.	60

Guideline for M. Tech Dissertation Phase-I

- Supervisors will we assigned by HOS/ HOD within one week from the start of semester.
- Candidates are required to finalize their dissertation topic in consultation to their assigned supervisor within 15 days after assignment of the supervisor.
- Every candidate has to submit a write-up to the supervisor within one month after finalization of topic in the following format –
    a) Title of dissertation
    b) Introduction
    c) Literature review
    d) Problem Definition
- Dissertation Work Review I :
  Every Candidate has to give a presentation on write-up, in consultation with his Supervisor to the **Dissertation Work Review Committee** (DWRC) for the approval on the topic.
- Dissertation Work Review Committee will be constituted under the chairmanship of HOS/ HOD, the composition of DWRC is as follows
    a) HOS/ HOD – Chairperson
    b) Two Senior Faculty members of concerned department
    c) Supervisor
- Every candidate is required to submit the synopsis to the supervisor within 12 weeks after the commencement of semester in the following format
    1. Title of dissertation
    2. Abstract
    3. Introduction and research significance
    4. Literature review
    5. Objectives
    6. Proposed methodology
    7. Expected outcomes
    8. References

    Guidelines for Synopsis

    1. All text must be in Times New Roman
    2. Headings (**Times New Roman, Bold, Text size=14**)
    3. Sub Headings (**Times New Roman, Bold, Text size=12**)
    4. Running Text (Times New Roman, Text size=12)

- Before the final submission of Dissertation phase-I the candidate has to publish at least one research paper, related to his/her area of research, in some reputed National/ International Journal/ Conference of repute.
- The candidate is required to submit the Dissertation Phase-I with the proof of publications.
- Furthermore, each candidate is required to give a certificate, duly signed by the candidate and counter signed by the supervisor, certifying that the dissertation of the candidate is free of any kind of plagiarism along with the report of plagiarism detection tool.
- The Dissertation phase -I Viva-Voce examination shall be conducted by a board consisting of the

Supervisor and the external examiner appointed by Controller of Examination of University.

- Distribution of internal marks for all the stages of Dissertation phase –I

Timely finalization of topic and submission of write-up	(15)
Power Point Presentation on topic and write-up	(15)
Submission of Synopsis and Presentation	(20)
Publication of Research Paper	(50)
Final Presentation and Submission of Dissertation Phase –I	(50)

Guideline for M. Tech Dissertation Phase – II

- After the successful completion of the Dissertation phase-I, a candidate can initiate the Dissertation phase-II work.
- Every Candidate has to give presentations before the DWRC on the work progress in consultation with his supervisor in fourth and eighth weeks after the commencement of semester.
- A candidate is permitted to submit thesis only after successful completion of all theory and practical courses with the approval of DWRC not earlier than 40 weeks from the date of approval of the dissertation topic.
- The candidate has to submit the draft copy of Dissertation-II to the HOD/ HOS for the approval of DWRC..
- The DWRC will examine the overall progress of the Dissertation Work and decide whether or not the Dissertation is eligible for final submission.
- If DWRC permits then candidate has to give presentation before the DWRC required for final submission of thesis.
- Publication of one research paper in fourth semester is mandatory in any one journal of UGC care/ SCOPUS /SCI.
- After approval from the DWRC, a soft copy of the thesis should be submitted for plagiarism check and the plagiarism report should be submitted to the University and be included in the final thesis. The Thesis will be accepted for submission, if the similarity index is less than 15%.
- If the similarity index has more than the required percentage, the candidate is advised to modify accordingly and re-submit the soft copy of the thesis after 15 days.
- Three copies of the Dissertation-II thesis certified by the supervisor shall be submitted to the HOS/HOD, one copy of the submitted research paper shall be attached to thesis.
- For this, the HOS shall submit a panel of three examiners from among the list of experts in the relevant specialization as submitted by the supervisor concerned and Head of the Department. If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unsatisfactory again, the thesis shall be summarily rejected. Subsequent actions for such dissertations may be considered, only on the specific recommendations of the DWRC. No further correspondence in this matter will be entertained, if there is no specific recommendation for resubmission.
- If the report of the examiner is satisfactory, the HOD/ HOS shall coordinate and make arrangements for the conduct of Dissertation Viva- Voce examination. The Dissertation Viva-Voce examination

shall be conducted by a board consisting of the Supervisor, HOD/ HOS and the external examiner who adjudicated the Thesis.

- If he fails to fulfill the requirements as specified in previous point he will reappear for the VivaVoce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree, unless he is asked to revise and resubmit his dissertation work by the board within a specified time period (within four years from the date of commencement of his first year first semester).
- Distribution of internal marks for all the stages of Dissertation Phase –II

First Power Point Presentation	(25)
Second Power Point Presentation	(25)
Publication of Research Paper	(50)
Final Presentation and Submission of Dissertation Phase –II	(100)